

<b>Notice of References Cited</b>	Application/Control No. 09/655,595	Applicant(s)/Patent Under Reexamination BEAUSOLEIL ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,504,841	01-2003	Larson et al.	370/386
	B	US-5,157,665	10-1992	Fakhraie-Fard et al.	714/712
	C	US-5,551,013	08-1996	Beausoleil et al.	703/23
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Mak et al. "Board-Level Multi-terminal Net Routing for FPGA-based Logic Emulation. 1997 ACM pg.152-167
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.